What is claimed is:

1. An apparatus for selectively converting a clock frequency in a digital signal receiver, comprising:

a first phase locked loop (PLL);

a second phase locked loop;

a switching portion for selecting a clock frequency from one of the first and second phase locked loops according to a predetermined control signal; and

a controller for controlling the switching portion to select and output the clock frequency corresponding to the frame rate of an input digital signal.

2. The apparatus of claim 1, wherein the first phase locked loop generates a clock frequency of 74.25 MHz and the second phase locked loop generates a clock frequency of 74.175 MHz.

3. The apparatus of claim 1, wherein when the frame rate of the input digital signal is 60 Hz, 30 Hz or 24 Hz, the controller controls the switching portion to select the clock frequency from the first phase locked loop, and when the frame rate of the input digital signal is 59.94 Hz, 29.97 Hz or 23.97 Hz, the controller controls the switching portion to select the clock frequency from the second phase locked loop.